Accelerating SRAM Design Cycles With Additive AI Technology

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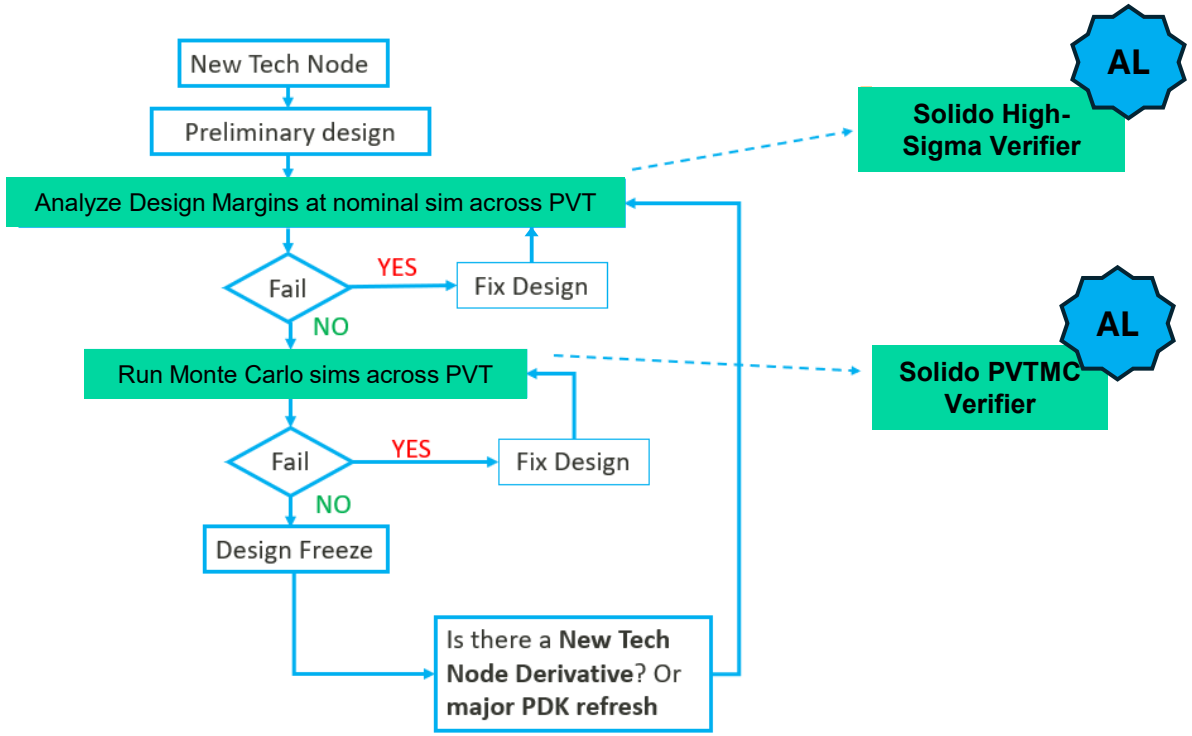
SRAM Verification Challenges

- SRAMs occupy nearly 40% of Mobile SoCs, hence crucial for chip yield
- Yield Qualification in SRAM
  - Bitcell – Need 6-sigma qualification
  - Periphery Logic – Need at least 4- to 4.5-sigma qualification
- Mobile SOCs are targeting lower V_{min} for each generation
  - Lower Voltage → Higher device variation
- Most design cycles are iterative with every failure, design change, technology update, etc.
- Brute Force Monte Carlo simulations are time- and compute-consuming
- We need a better solution that meets our performance and accuracy requirements

Solution: AI-powered methodology to retain and reuse models with iterative workflows

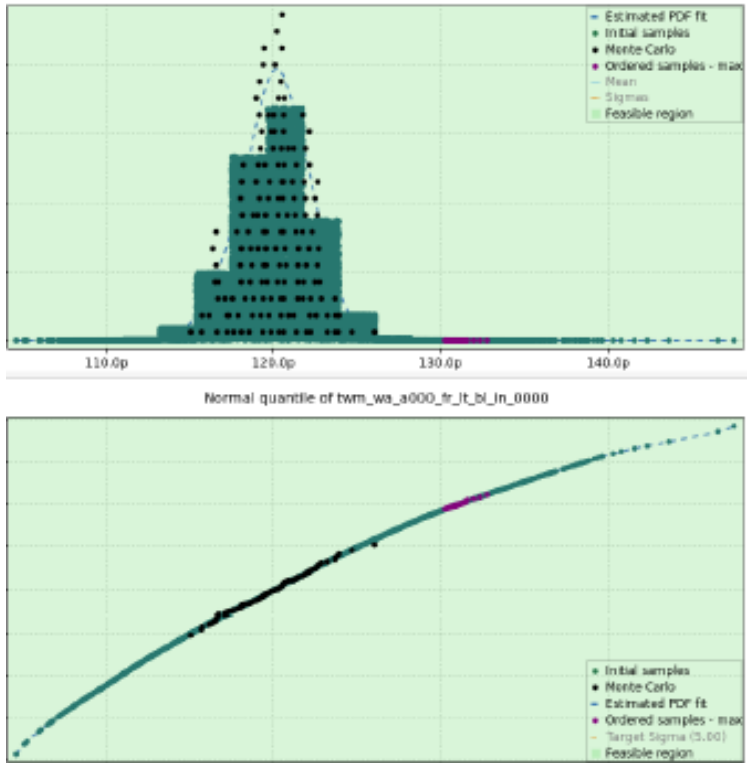
- A Solido-based methodology is being used
- The design cycle is iterative
  - When a failure is found, the design needs to be fixed and re-run
  - Design changes and tech updates also require a re-run
  - Multiple iterations are executed, taking up valuable time and resources
- Solido Additive Learning technology was used to reduce simulations for each iteration
  - Saves data/models from previous jobs to reduce simulations for subsequent runs



Solution: AI-powered methodology to retain and reuse models with iterative workflows

Solido High-Sigma Verifier

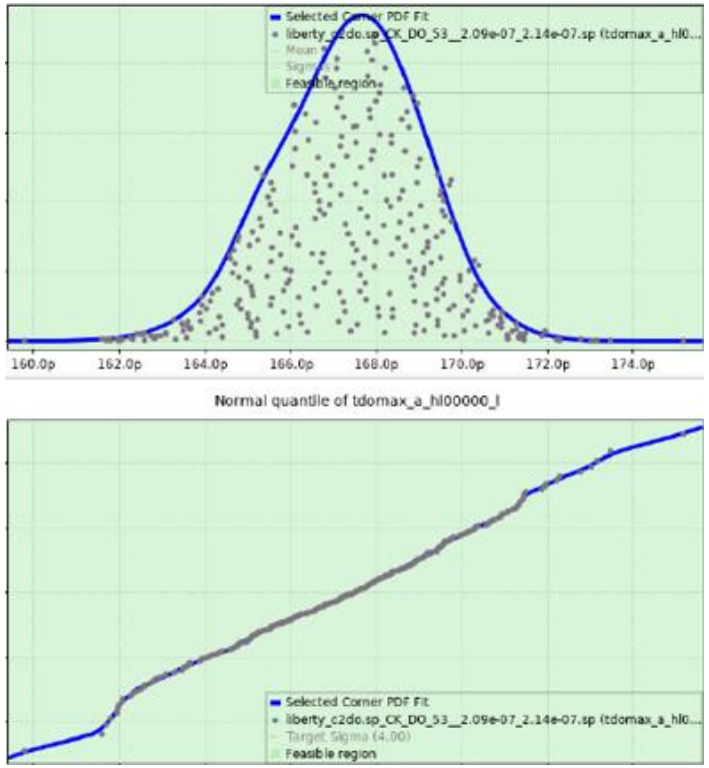
- Verifiable brute-force accurate high-sigma verification
  - E.g., 6-sigma yield verification in only 1,000s of simulations
- 1,000-1,000,000,000x+ faster than brute-force, while maintaining full SPICE accuracy
  - Brute-force MC sample populations verify to within +/- 0.1-sigma
- Verified answers with no assumptions



Solution: AI-powered methodology to retain and reuse models with iterative workflows

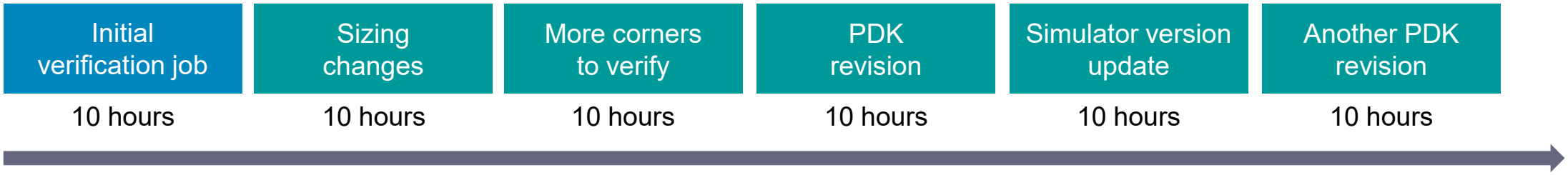
Solido PVTMC Verifier

- Full coverage verification across PVT corners + Monte Carlo
  - Covers all PVTs in a single run
- 2-10x+ faster than traditional approaches
- Finds problems that can't be found without massive simulation
  - Quickly finds outliers other methods can't
- No extrapolation or Gaussian assumptions



AI-powered methodology reuses results from previous jobs to save on each iteration

Traditional verification workflow:

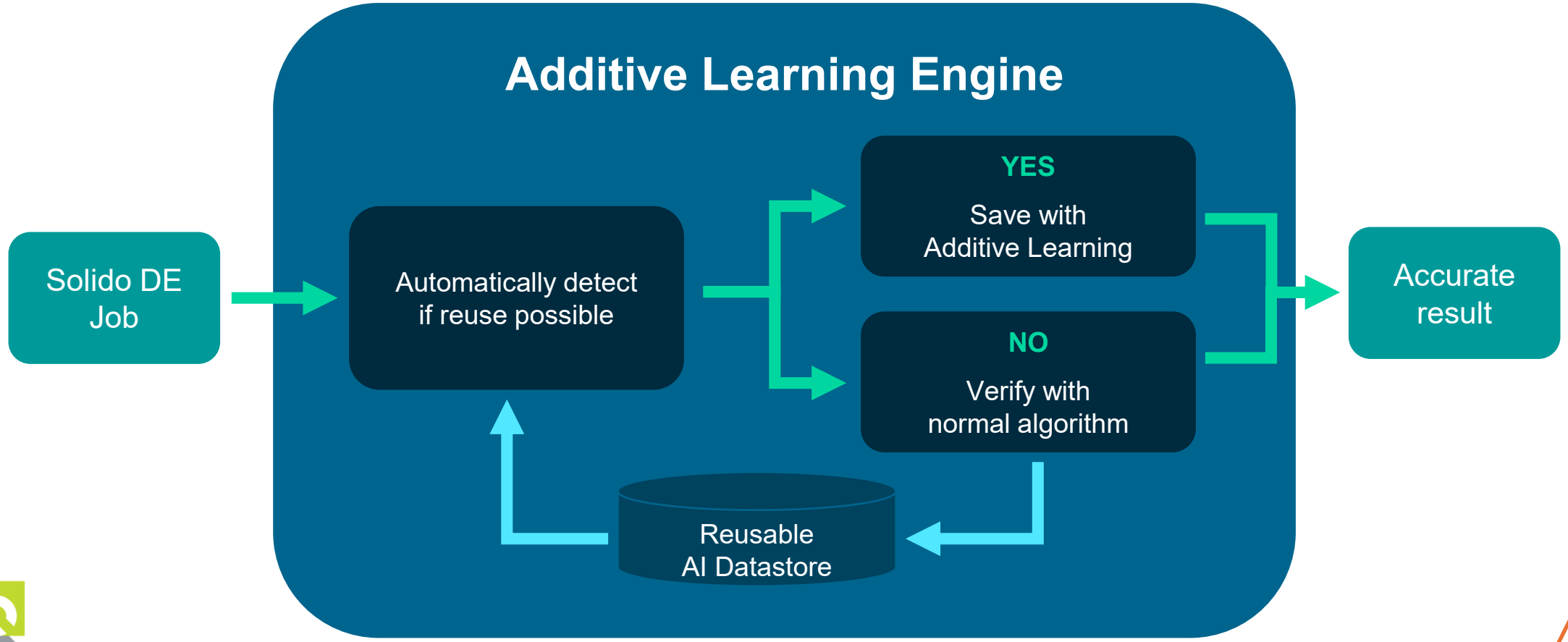


Total time for 5 iterations: 50 hours

Additive Learning iterative workflow:

Total time for 5 iterations: 5 hours

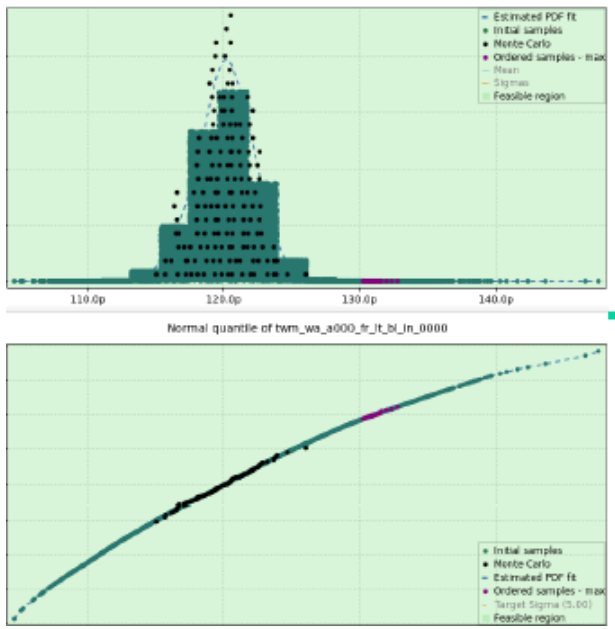
Solido Additive Learning Algorithm



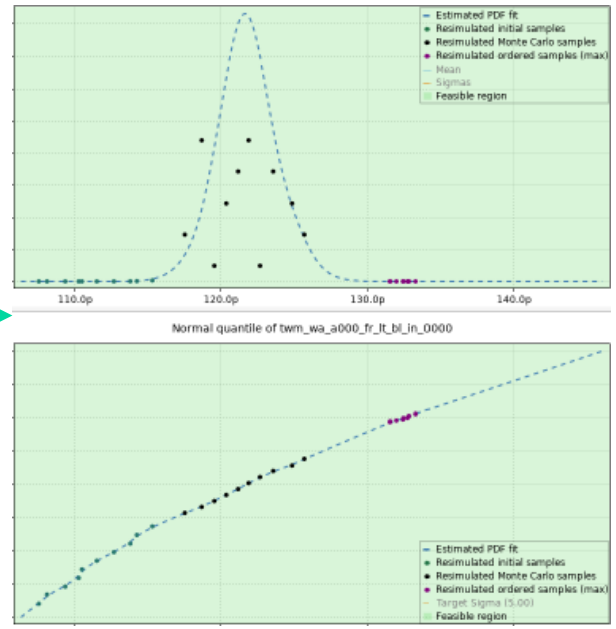
Results showing 67X speedup with verified accuracy

- **Case 1:** 5-sigma bitcell write margin (CK to bitcell flip) verified using Solido High-Sigma Verifier
- **Base run results:**
  - Mean = 120.1ps; 5-sigma = 131.2ps
  - **No. of simulations = 2,500**
- **Additive Learning run after a design fix** (V_t changed for Write driver and Col-Mux)**:**
  - Mean = 121.8ps; 5-sigma = 132.5ps
  - **No. of simulations = 29**
  - **Simulation Speedup – 67X**

Base run

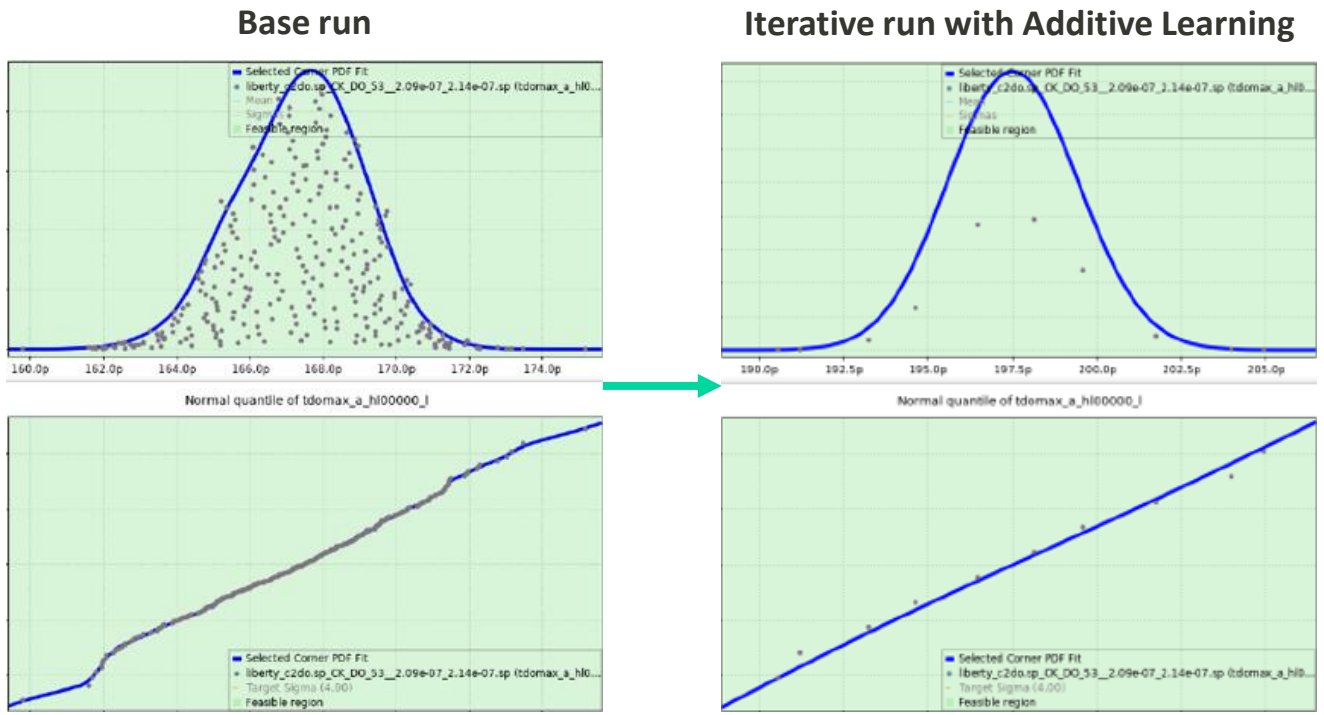


Iterative run with Additive Learning



Results showing 20X speedup with verified accuracy

- **Case 2:** 4-sigma for instance level (CK to DO) verified using Solido PVTMC Verifier
- **Original run results:**
  - Mean = 167.4ps; 4-sigma = 173.1ps
  - **No. of simulations = 300**
- **Additive Learning run after design fix** (V_t update for Control/IO blocks: ULVT replaced with LVT):
  - Mean = 198ps; 4-sigma = 204.6ps
  - **No. of simulations = 15**
  - **Simulation Speedup – 20X**
- **Double checked by running fixed design without AL:**
  - Mean = 198ps; 4-sigma = 204.8ps



Summary

Challenge: SRAM Yield qualifications are challenging, and design cycle is iterative

Solution: Solido Additive Learning for iterative jobs

- Reusing models from previous runs to significantly save simulations
  - PDK revisions, sizing changes, tool version updates, adding more corners, etc.

⚡ **Fast**: Re-use AI results from previous jobs to save on each iteration

🎯 **Accurate**: Equivalent to full verification job

🧠 **Automatic**: AI constantly tracks and makes decisions

Results of re-verification iterations:

- Testcase 1 (BITCELL): **67X additional speedup** with verified accuracy
- Testcase 2 (SRAM instance level): **20X additional speedup** with full accuracy

Thank you!

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